REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on July 30, 2003, and the references cited therewith.

Claims 1, 6, 13, and 18 are amended, no claims are canceled, and no claims are added; as a result, claims 1-50 remain pending in this application.

§103 Rejection of the Claims

Claims 1-5 and 13-17 were rejected under 35 USC § 103(a) as being unpatentable over Rengarajan et al. (U.S. Patent No. 6,323,103) in view of Choi et al. (U.S. Patent No. 5,750,424) and Komori et al. (U.S. Patent No. 5,455,437). Claims 6-12 and 18-24 were rejected under 35 USC § 103(a) as being unpatentable over Rengarajan et al. in view of Komori et al.

Applicant does not admit that adequate motivation or teaching can be found within the Kumori reference for a proper combination with Rengarajan or Choi. Nevertheless, Applicant submits that even if properly combined, Kumori is distinguished from the present claims as discussed below.

The rejection states that, "Rengarajan et al. in view of Choi et al. fail to teach that a well of opposite conductivity lies below the well of first conductivity." The rejection further states that Komori et al. teach a method of forming a well of one conductivity below a well of an opposite conductivity and it would have been obvious to combine Komori with Rengarajan and Choi.

Komori appears to show a p-well 4 in an n-well 6. Komori further appears to show a separate n-well 5 adjacent to the p-well 4. Komori appears to utilize a number of masking steps [Figures 7(a) - 7(d)] in the formation of the number of wells. Komori does not show forming a first conductivity type semiconductor well in the first conductivity type well region, the first conductivity well region being located over a portion of a second conductivity type semiconductor well, wherein the **second conductivity type semiconductor well is sized to accommodate at least one transistor outside the first conductivity well portion**. Further, Komori does not show patterning and forming gates wherein a first gate is formed over the first conductivity type semiconductor well, and a second gate is formed over a **remaining portion** of the second conductivity type semiconductor well.

In contrast, claims 1 and 6, as amended, include forming a first conductivity type semiconductor well in the first conductivity type well region, the first conductivity well region being located over a portion of a second conductivity type semiconductor well, wherein the second conductivity type semiconductor well is sized to accommodate at least one transistor outside the first conductivity well portion. Further in contrast, claims 13 and 18, as amended, include patterning and forming gates wherein a first gate is formed over the first conductivity type semiconductor well, and a second gate is formed over a remaining portion of the second conductivity type semiconductor well.

Applicant's specification discusses disadvantages of using a number of masks on page 2, lines 12-17. Applicant's specification further discusses advantages of claimed configurations such as a reduction in a number of masks on page 9, lines 21-30.

Because the cited references, either alone or in combination, do not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 1, 6, 13, and 18. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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Date 10-30-2003

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30 day of October, 2003.

Tina Kohut
Name

Signature